REMARKS

1. Amendments to the specification:

The specification is amended in accordance with the drawing. No new matter is introduced. Allowance of the amendments in the specification is hereby requested.

2. Rejection of claims 1-3 under 35 U.S.C. 102(b):

Claims 1-3 are rejected under 35 U.S.C. 102(b), for reasons of record that can be found on pages 2-3 in the Office action identified above.

Response:

Claims 2-3 are merged into claim 1 to overcome the rejections presented by the Examiner, and claims 2-3 are thereby canceled. The limitation "*a capacitance of each of the compensating capacitors is increased when a distance between the pixels and the first input end of the second scanning line is increased*" of the original claim 3 is replaced by "*the larger a distance between the first input end of the second scanning line and a corresponding one of the plurality of pixels is, the larger a capacitance of the compensating capacitor of the corresponding pixel is*". Support for the amended claim 1 can be found in the written description as filed in paragraphs [0031]-[0032]. No new matter has been introduced by this amendment.

The amended claim 1 is repeated below, in clean format, for reference:

"1.A liquid crystal display panel comprising:

an upper substrate;

a lower substrate;

a plurality of pixels located between the upper substrate and the lower substrate;

a first scanning line;

a second scanning line; and

a scanning line driving circuit, each of the pixels being located between the first scanning line and the second scanning line and having at least a compensating capacitor for providing an approximately identical feed-through voltage for each of the pixels, each of the first scanning line and the second scanning line having a first input end so that the scanning line driving circuit can input signals into the first scanning line and the second scanning line through the first input ends;

wherein **the larger a distance between the first input end of the second scanning line and a corresponding one of the plurality of pixels is, the larger a capacitance of the compensating capacitor of the corresponding pixel is.**"

As described in the amended claim 1 and Fig.4 of the present application, the capacitance of the compensating capacitor C (i.e. C_A, C_B, and C_C in Fig. 4) is in accordance with the distance between the pixel and the first input end of the second scanning line. In other words, **the capacitance of the compensating capacitor of the pixel is varied with the position of the pixel.** The greater the distance between the pixel and the first input end of the

second scanning line is, the larger the capacitance of the compensating capacitor of the pixel is. It means that $C'_A<C'_B<C'_C$ as long as $D_A<D_B<D_C$, where C'_A, C'_B, and C'_C respectively represent the capacitances of the compensating capacitors C_A, C_B, and C_C of the pixels A, B, and C, and D_A, D_B, and D_C respectively represent the distances between the first input end of the second scanning line GL_1 and the pixels A, B, and C.

The Examiner rejected the original claim 3 under U.S.C. 102(b) as anticipated by Yanai et al. Yanai et al. disclose that the display electrode 3 is provided with a variable compensation capacitor 6 to compensate for a potential fluctuation occurring in the display electrode after the gate of the thin film transistor 2 is selected (col.7, lines 39-43). Further, Yanai et al. disclose that **the capacitance of the variable compensation capacitor 6** of the active matrix liquid crystal display apparatus, in Figs. 5B and 5C, **increases during a period Tb** for compensating a DC voltage level shift and **decreases during a storage period Ta** other than the period Tb (col.7, lines 50-59). During the period Ta, the gate of the thin film address transistor 2 is not selected. Since the variable compensation capacitor 6 has a large capacitance during the compensation period Tb, it can reduce the compensation voltage.

However, Yanai et al. fails to disclose that the greater the distance between the corresponding pixel and the first input end of the second scanning line is, the larger the capacitance of the compensating

capacitor of the corresponding pixel is. Thus, the amended claim 1 is patentably distinguishable from Yanai et al.

3. Rejection of claims 5 and 13 under 35 U.S.C. 102(b) :

Claims 5 and 13 are rejected under 35 U.S.C. 102(b), for reasons of record that can be found on pages 3-4 in the Office action identified above.

Response:

As described in the claims 5 and 13, each of the compensating capacitors is composed of an overlapping region, which **is formed by overlapping the corresponding pixel electrode over the scanning line.**

The Examiner rejected the claims 5 and 13 under U.S.C. 102(b) as anticipated by Yanai et al. The Examiner suggested that Yanai et al. discloses an apparatus, wherein each of the compensating capacitor 6 is composed of a first overlapping region S1. However, the first overlapping region S1 is formed by overlapping the upper electrode 61 over the semiconductor layer 63 (col.10, lines 51-52), **not** formed by overlapping the pixel electrode over the scanning line. Therefore, the claims 5 and 13 are patentably distinguishable from Yanai et al. Moreover, the claims 5 and 13 are dependent upon the amended claim 1 and should be allowed if the amended claim 1 is allowed.

4. Rejection of claim 6 under 35 U.S.C. 102(b) :

Claim 6 is rejected under 35 U.S.C. 102(b), for

reasons of record that can be found on page 3 in the Office action identified above.

Response:

Claim 6 has been amended to overcome the rejection presented by the Examiner. No new matter has been introduced by this amendment. Support for the amended claim 6 can be found in the written description as filed in paragraph [0037].

As described in the amended claim 6 and Fig.5A of the present application, the area of the first overlapping region (i.e. 70a, 70b, or 70c in Fig.5A) of each of the pixels A, B, and C is in accordance with the distance between the pixel and the first input end of the first scanning line. In other words, the area of the first overlapping region of the pixel is varied with the position of the pixel. The greater the distance between the pixel and the first input end of the first scanning line is, the larger the area of the first overlapping region of the pixel is. It means that $A_A<A_B<A_C$ as long as $D_A<D_B<D_C$, where A_A, A_B, and A_C respectively represent the areas of the first overlapping areas 70a, 70b, and 70c of the pixels A, B, and C, and D_A, D_B, and D_C respectively represent the distances between the first input end of the first scanning line GL_0 and the pixels A, B, and C.

However, Yanai et al. fails to disclose this above-mentioned feature as recited in the amended claim 6. Thus, the amended claim 6 is patentably distinguishable from Yanai et al. Moreover, the

amended claim 6 is dependent upon the amended claim 1 and should be allowed if the amended claim 1 is allowed.

5. Rejection of claim 7, 15, and 26 under 35 U.S.C. 102(b):

Yanai et al. teaches an apparatus, wherein each of the compensating capacitor 6 is composed of a second overlapping region S2, which is formed by overlapping the corresponding source electrode over the corresponding gate electrode (col.10, lines 26+)

Response:

According to the amended claim 1, claims 4, 7, and Fig. 6 of the present application, each of the pixels has a **thin film transistor** which has a gate electrode, drain electrode, and a source electrode. Each of the second overlapping regions (68a, 68b, and 68c) is formed by overlapping the source electrode (64a, 64b, or 64c) of the corresponding **thin film transistor (TFT)** (T_A, T_B, or T_C) over the gate electrode (60a, 60b, or 60c) of the corresponding **thin film transistor** (T_A, T_B, or T_C).

The Examiner rejected the claim 7 under U.S.C. 102(b) as anticipated by Yanai et al. Yanai et al. disclose that the variable compensation capacitor 6 has a laminated **MIS** structure comprising, from the top to the bottom in FIG. 8B, an upper electrode 61, an insulation layer 62, a semiconductor layer 63, and a lower electrode 64. The lower electrode 64 comprises an ohmic contact portion 641 that is

electrically connected to the semiconductor layer 63, and an electrode portion 642. The area S2 is formed by overlapping the upper electrode 61 over the lower electrode 64. However, the MIS structure is not a thin film transistor (TFT). Therefore, Yanai et al. fails to disclose that each of the second overlapping regions is formed by overlapping the source electrode of the corresponding thin film transistor over the gate electrode of the corresponding thin film transistor. Thus, claim 7 is patentably distinguishable from Yanai et al.

Claims 15 and 26 have similar features as claim 7 and are patentable for the same reason set forth. Therefore, consideration of claims 15 and 26 is respectfully requested.

6. Rejection of claims 8 and 16 under 35 U.S.C. 102(b) :

Claims 8 and 16 are rejected under 35 U.S.C. 102(b), for reasons of record that can be found on page 4 in the Office action identified above.

Response:

Claims 8 and 16 have been amended to overcome the rejection presented by the Examiner. No new matter has been introduced by this amendment. Support for the amended claims 8 and 16 can be found in the written description as filed in paragraphs [0037] and [0042].

As described in the amended claim 8 and Fig.6 of the present application, the area of the second

overlapping region (i.e. 68a, 68b, or 68c in Fig.6) of each of the pixels A, B, and C is in accordance with the distance between the pixel and the first input end of the first scanning line. In other words, the area of the second overlapping region of the pixel is varied with the position of the pixel. The greater the distance between the pixel and the first input end of the first scanning line is, the larger the area of the second overlapping region of the pixel is. It means that $A2_A<A2_B<A2_C$ as long as $D_A<D_B<D_C$, where $A2_A$, $A2_B$, and $A2_C$ respectively represent the areas of the second overlapping areas 68a, 68b, and 68c of the pixels A, B, and C, and D_A, D_B, and D_C respectively represent the distances between the first input end of the first scanning line GL_0 and the pixels A, B, and C.

However, Yanai et al. fails to disclose this above-mentioned feature as recited in the amended claim 8. Thus, the amended claim 8 is patentably distinguishable from Yanai et al. Moreover, the amended claim 8 is dependent upon the amended claim 1 and should be allowed if the amended claim 1 is allowed.

The amended claim 16 has similar features as the amended claim 8 and is patentable for the same reason set forth. Therefore, consideration of the amended claim 16 is respectfully requested.

7. Rejection of claims 9 and 17 under 35 U.S.C. 102(b) :

Claims 9 and 17 are rejected under 35 U.S.C. 102(b),

for reasons of record that can be found on page 4 in the Office action identified above.

Response:

Claims 9 and 17 have been amended to overcome the rejection presented by the Examiner. No new matter has been introduced by this amendment. Support for the amended claims 9 and 17 can be found in the written description as filed in paragraphs [0034] and [0046].

As described in the amended claim 9 and Fig.4 of the present application, the capacitance of the storage capacitor of each of the pixels A, B, and C is in accordance with the distance between the pixel and the first input end of the scanning line. **The greater the distance between the pixel and the first input end of the scanning line is, the smaller the capacitance of the storage capacitor of the corresponding pixel is.** It means that $C_{SCA}>C_{SCB}>C_{SCC}$ as long as $D_A<D_B<D_C$, where C_{SCA}, C_{SCB}, and C_{SCC} respectively represent the capacitances of the storage capacitors of the pixels A, B, and C, and D_A, D_B, and D_C respectively represent the distances between the first input end of the scanning line GL_0 and the pixels A, B, and C.

However, Yanai et al. fails to disclose the feature as recited in the amended claim 9. Thus, the amended claim 9 is patentably distinguishable from Yanai et al. Claim 17 has similar features as claim 9 and is patentable for the same reason set forth. Moreover, the amended claims 9 and 17 are dependent upon the

amended claim 1 and should be allowed if the amended claim 1 is allowed.

8. Rejection of claims 11 and 14 under 35 U.S.C. 102(b):

Claim 11 is rejected under 35 U.S.C. 102(b), for reasons of record that can be found on pages 3-4 in the Office action identified above.

Response:

Claims 11 and 14 have been amended to overcome the rejection presented by the Examiner. No new matter has been introduced by this amendment. Support for the amended claims 11 and 14 can be found in the written description as filed in paragraphs [0048]-[0050].

As described in the amended claims 11, 14 and Fig.8 of the present application, the overlapping regions 100a, 100b, and 100c respectively correspond to the compensating capacitors C_A, $C_{B'}$, and $C_{C'}$ of the pixels A, B', and C'. The area of the overlapping region (i.e. 100a, 100b, or 100c in Fig.8) of each of the pixels A, B', and C' is in accordance with the distance between the pixel and the second input end of the data line. In other words, the area of the overlapping region 100a, 100b, or 100c of the corresponding pixel A, B', or C' is varied with the position of the pixel. The greater the distance between the corresponding pixel and the second input end of the data line is, the larger the area of the overlapping region of the pixel is. It means that $A_A<A_{B'}<A_{C'}$ as long as $D_A<D_{B'}<D_{C'}$, where A_A, $A_{B'}$, and

$A_{C'}$ respectively represent the areas of the overlapping areas 100a, 100b, and 100c of the pixels A, B', and C', and D_A, $D_{B'}$, and $D_{C'}$ respectively represent the distances between the second input end of the data line 86a or 86b and the pixels A, B', and C'. Because $A_A<A_{B'}<A_{C'}$, the compensating capacitor of the pixel B' is greater than the compensating capacitor of the pixel A but less than the compensating capacitor of the pixel C'. Therefore, the larger a distance between the corresponding pixel and the second input end is, the larger a capacitance of the compensating capacitor of the corresponding pixel is.

However, Yanai et al. fails to disclose the feature as recited in the amended claims 11 and 14. Thus, the amended claims 11 and 14 are patentably distinguishable from Yanai et al. Moreover, the amended claims 11 and 14 are dependent upon the amended claim 1 and should be allowed if the amended claim 1 is allowed.

9. Rejection of claims 4, 10, and 12 under 35 U.S.C. 102(b) :

Claims 4, 10, and 12 are rejected under 35 U.S.C. 102(b), for reasons of record that can be found on pages 3-5 in the Office action identified above.

Response:

Claim 3 has been canceled. Therefore, claim 4 has been amended so that it is now dependent upon claim 1.

Claims 4, 10, and 12 are patentably distinguishable

from Yanai et al. by reason of their dependence upon the amended claim 1, as well as its recitation. Hence, the Applicants submit that each of these dependent claims is not anticipated in view of Yanai et al.

10. Rejection of claim 18 under 35 U.S.C. 102(b):

Claim 18 is rejected under 35 U.S.C. 102(b), for reasons of record that can be found on page 5 in the Office action identified above.

Response:

Claim 18 has been amended to overcome the rejection presented by the Examiner. No new matter has been introduced by this amendment. Support for the amended claim 18 can be found in the written description as filed in paragraph [0032].

The amended claim 18 is repeated below, in clean format, for reference:

"18. A liquid crystal display panel comprising:

a plurality of scanning lines, each of the scanning lines having at least one signal input end;

a plurality of data lines, each of the data lines having at least one signal input end; and

a plurality of pixels, each of the pixels having a pixel electrode, and a thin film transistor having a gate electrode connected to the corresponding scanning line, a drain electrode connected to the corresponding data line, and a source electrode connected to the

pixel electrode, wherein a first overlapping region is formed by overlapping the pixel electrode over the corresponding scanning line; wherein **the larger a distance between one of the signal input ends and a corresponding one of the pixels is, the greater an area of the corresponding first overlapping region is.**

As described in the amended claim 18 and Figs. 4-5A of the present application, the capacitance of the compensating capacitor C(i.e. C_A, C_B, and C_C in Fig. 4) is in accordance with the distance between the pixel and the signal input end. In other words, the capacitance of the compensating capacitor of the pixel is varied with the position of the pixel. The greater the distance between the pixel and the signal input end is, the larger the capacitance of the compensating capacitor of the pixel is. It means that $C'_A<C'_B<C'_C$ as long as $D_A<D_B<D_C$, where C'_A, C'_B, and C'_C respectively represent the capacitances of the compensating capacitors C_A, C_B, and C_C of the pixels A, B, and C, and D_A, D_B, and D_C respectively represent the distances between the first input end of the second scanning line GL_1 and the pixels A, B, and C. The compensating capacitors C_A, C_B, and C_C respectively correspond to the overlapping regions 70a, 70b, and 70c shown in Fig.5. Since the compensating capacitors C_A, C_B, and C_C are increased sequentially, the area of the overlapping region 70a is smaller than the area of the overlapping region 70b, whose area is smaller than that of the overlapping region 70c (i.e. 70a<70b<70c).

The Examiner rejected the original claim 18 under U.S.C. 102(b) as anticipated by Yanai et al. Yanai et al. discloses an apparatus comprising a plurality scanning lines 11 & 12; a plurality of data lines 5; and a plurality of pixels/TFT 2, each of the pixels having a pixel electrode 84a, and a thin film transistor 83 having a gate electrode 85 connected to the corresponding scanning line 11/12, a drain electrode 86 connected to the corresponding data line 5, and a source electrode 86 connected to the pixel electrode (col.5, lines 25+), wherein a first overlapping region S1 is formed by overlapping the pixel electrode over the corresponding scanning line 11/12.

However, Yanai et al. fails to disclose that the greater the distance between the corresponding pixel and the signal input end is, the greater the area of the overlapping region S1 is. There is no relationship between the position of the pixel and the area of the overlapping region S1. Thus, the amended claim 18 is patentably distinguishable from Yanai et al.

11. Rejection of claims 19-29 under 35 U.S.C. 102(b):

Claims 19-29 are rejected under 35 U.S.C. 102(b), for reasons of record that can be found on pages 3-4, 6 in the Office action identified above.

Response:

The claims 24-25 are amended to simplify the

limitations recited. Claims 28-29 are amended according to the paragraphs [0032] and [0043]. No new matter has been introduced by this amendment.

Claims 19-29 are patentably distinguishable from Yanai et al. by reason of their dependence upon the amended claim 18, as well as its recitation. Hence, the Applicants submit that each of these dependent claims is not anticipated in view of Yanai et al.

12. Rejection of claims 30 and 34 under 35 U.S.C. 102(b):

Claims 30 and 34 are rejected under 35 U.S.C. 102(b), for reasons of record that can be found on pages 6-7 in the Office action identified above.

Response:

As described in the claims 30 and 34, the first overlapping region is formed by overlapping the first pixel electrode over the scanning line, and the second overlapping region is formed by overlapping the second pixel electrode over the scanning line. Therefore, **the first overlapping region and the second overlapping region of the present application are formed by overlapping the scanning line over two different pixel electrodes.** Moreover, because the first region is located between the scanning line driving circuit and the second region, the first overlapping region is located between the scanning line driving circuit and the second overlapping region, where the area of the second overlapping region is larger than the area of the first overlapping region. It means that D1<D2 and

A1<A2, where D1 and D2 respectively represent the distances between the scanning line driving circuit and the two overlapping regions, and A1 and A2 respectively represent the areas of the first overlapping region and the second overlapping region.

The Examiner rejected the claims 30 and 34 under U.S.C. 102(b) as anticipated by Yanai et al. However, Yanai et al. disclose an apparatus comprising a second overlapping region S2 being formed by overlapping the upper electrode 61 over the lower electrode 64 (col.10, lines 56-57), and a first overlapping region S1 being formed by overlapping the upper electrode 61 over the semiconductor layer 63 (col.10, lines 51-52). It is obvious that the first overlapping region S1 **is not** formed by overlapping the scanning line over the upper electrode 61. Moreover, Yanai et al. never disclose the relationship between ***the area of the second overlapping region S2*** and ***the distance between the scanning line driving circuit and the second overlapping region S2***. Thus, the claims 30 and 34 are patentably distinguishable from Yanai et al.

13. Rejection of claims 31-33, 35-37 under 35 U.S.C. 102(b):

Claims 31-33, 35-37 are rejected under 35 U.S.C. 102(b), for reasons of record that can be found on pages 4 and 7 in the Office action identified above.

Response:

Claims 36-37 are amended according to the paragraphs [0036]-[0041]. No new matter has been

introduced by this amendment.

Claims 31-33, 35-37 are patentably distinguishable from Yanai et al. by reason of their dependence upon the claim 30 or 34, as well as its recitation. Hence, the Applicants submit that each of these dependent claims is not anticipated in view of Yanai et al.

14. Rejection of claims 38-39 under 35 U.S.C. 102(b):

Claims 38-39 are rejected under 35 U.S.C. 102(b), for reasons of record that can be found on pages 3, 7-8 in the Office action identified above.

Response:

Claim 39 is merged into claim 38 to overcome the rejections presented by the Examiner, and claim 39 is thereby canceled. The limitation "*a capacitance of each of the compensating capacitors is increased as a distance between each of the pixels and the scanning line driving circuit is increased*" of the original claim 39 is replaced by "*the larger a distance between the scanning line driving circuit and a corresponding one of the pixels is, the greater a capacitance of the compensating capacitor of the corresponding pixel is*". Support for the amended claim 38 can be found in the written description as filed in paragraphs [0031]-[0032] and [0038]. No new matter has been introduced by this amendment.

The amended claim 38 is repeated below, in clean format, for reference:

"38. A liquid crystal display panel comprising:

a plurality of scanning lines for transmitting scanning signals from a scanning line driving circuit;

a plurality of data lines for transmitting image signals from a data line driving circuit; and

a plurality of pixels, each of the pixels comprising:

a liquid crystal capacitor;

a thin film transistor electrically connected to the corresponding scanning line, the corresponding data line, and the liquid crystal capacitor; and

a compensating capacitor electrically connected between the liquid crystal capacitor and the corresponding scanning line, being connected to the thin film transistor, for providing an approximately identical feed-through voltage for each of the pixels;

wherein **the larger a distance between the scanning line driving circuit and a corresponding one of the pixels is, the greater a capacitance of the compensating capacitor of the corresponding pixel is.**

As described in the amended claim 38 and Figs. 4-5A of the present application, the capacitance of the compensating capacitor C (i.e. C_A, C_B, and C_C in Fig. 4) is in accordance with the distance between the pixel and the scanning line driving circuit. In other

words, the capacitance of the compensating capacitor of the pixel is varied with the position of the pixel. The greater the distance between the pixel and the scanning line driving circuit is, the larger the capacitance of the compensating capacitor of the pixel is. It means that $C'_A<C'_B<C'_C$ as long as $D_A<D_B<D_C$, where C'_A, C'_B, and C'_C respectively represent the capacitances of the compensating capacitors C_A, C_B, and C_C of the pixels A, B, and C, and D_A, D_B, and D_C respectively represent the distances between the scanning line driving circuit and the pixels A, B, and C.

However, Yanai et al. fails to disclose that the greater the distance between the scanning line driving circuit and the corresponding pixel is, the greater a capacitance of the compensating capacitor of the corresponding pixel is. There is no relationship between the position of the pixel and the compensating capacitor of the pixel. Thus, the amended claim 38 is patentably distinguishable from Yanai et al.

15. Rejection of claims 40-43 under 35 U.S.C. 102(b):

Claims 40-43 are rejected under 35 U.S.C. 102(b), for reasons of record that can be found on pages 4 and 8 in the Office action identified above.

Response:

Claim 41 is amended according to the paragraphs [0025]-[0026]. The claims 40, 42-43 are amended to simplify the limitations recited. No new matter has

been introduced by this amendment.

The amended claims 40-43 are patentably distinguishable from Yanai et al. by reason of their dependence upon the amended claim 38, as well as its recitation. Hence, the Applicants submit that each of these dependent claims is not anticipated in view of Yanai et al.

Respectfully submitted,

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